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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,448	10/26/2004	Hiroshi Takahara	260595US2PCT	4259

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EXAMINER	
ABDIN, SHAHEDA A	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
12/22/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/511,448	TAKAHARA ET AL.	
	Examiner	Art Unit	
	SHAHEDA A. ABDIN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-12 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-12 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The correspondence field on 09/25/2009 has been entered and considered by Examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 16 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For Example, the limitations "base anode line being arranged in a **free space**" have been recited in claim 16 which was not described in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10,12, 15-16, 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US Patent 6274887) in view of Yamazaki (US Patent No: 6765549) .

Regarding claim 10:

Yamazaki ('4887) in Fig. 29 A-B, discloses an EL display apparatus comprising: a substrate -that contains a display area panel having pixels arranged in a matrix, each pixel including an EL element (i.e. 5007) (column 34, lines 30-67, and Fig. 29 B);

a source driver IC (TFT 5002, Fig. 29 A) configured to apply a programming current or voltage to the pixels (column 34, lines 3037, and Fig. 29 B);

a first wiring (i.e. 5003) formed on the substrate and located under the source driver IC (TFT 5002);

a second wiring (i.e. 5001) electrically connected to the first wiring (5001) and formed between the source driver IC (5002) and a display area (i.e. pixel area);

Node that Yamazaki ('4887) does not clearly discloses an anode wiring branching from the second wiring and configured to applies an anode voltage to the pixels in the display area, a current being supplied to the EL elements via the anode wiring.

However, Yamazaki ('5549) discloses an anode wiring (anode wiring for EL element in Fig. 2) branching from the second wiring (G2) and configured to applies an anode voltage to the pixels in the display area, a current (current through the TFT) being supplied to the EL elements via the anode wiring (see Fg. 2, column 8 and lines 58-64).

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the method of anode wiring as taught by Yamazaki ('5554) in to the driving circuit of Yamazaki ('4887), so that an anode wiring could be branching from the second wiring and configured to applies an anode voltage to the pixels in the display area, a current could be supplied to the EL elements via the anode wiring. In this configuration the system would provide a high efficient EL device with preventing the decrease in the brightness of an EL element (Yamazaki ('5554) column 4, lines 10-13).

Regarding claim 12:

Yamazaki ('4887) further discloses driver transistors configured to supply light-emitting currents to the respective pixels and the driver transistors being P-channel transistors , and the TFT could being P channel, and transistors configured to generate the programming current in the source driver IC being N-channel transistors (column 30, lines 19-29, Fig. 25 B, and column 34, lines 38-55).

(1) Regarding claim 15 :

Yamazaki ('4887) in Fig. 19 A-B discloses an EL display apparatus with a display panel on which pixels, each including an EL element (5007), are placed in a matrix on a substrate, the EL display apparatus (column 34, lines 30-67, and Fig. 29 B);
) comprising:

a driver IC chip including a source driver circuit (i.e. TFT 5002, Fig. 29 A) placed on the substrate and configured to output a programming current or voltage to the pixels (column 34, lines 3037, and Fig. 29 B);

Yamazaki ('5549) discloses a supply line (anode supply line) configured to supply a current or voltage to the pixels, at least part of the supply line being arranged between the substrate and the driver IC chip (i.e. TFT 5002) ; and wiring (anode wiring) that branches from a supply line (G2) and extends to the pixels (),

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the method of supply line and wiring that brances from a supply line as

taught by Yamazaki ('5554) in to the driving circuit of Yamazaki ('4887), so that a supply line could be configured to supply a current or voltage to the pixels, at least part of the supply line being arranged between the substrate and the driver IC chip ; and

a wiring could be branching from a supply line which could be extended to the pixel. In this configuration the system would provide a high efficient EL device with preventing the decrease in the brightness of an EL element (Yamazaki ('5554) column 4, lines 10-13).-

(2) Regarding claim 16:

Yamazaki ('5549) wherein the supply line is an anode supply line having a base anode line (anode wiring), at least part of the base anode line being arranged in a free space between the substrate and the driver IC chip (TFT in the pixel), a common anode line placed between the driver IC chip and a display area, and at least one connection anode line connecting the base anode line to the common anode line (column 9, lines 1-27, Fig. 3).

(3) Regarding claim 18 :

Yamazaki ('4887) discloses a switch circuit (i.e. Switching TFT 4102, Fig. 26) arranged in an output stage of the source driver circuit and configured to turn on and off an output of the programming current or voltage (column 31, lines 30-50).

(4) Regarding claim 19:

Yamazaki ('4887) further discloses the pixel includes a driver transistor (5005, Fig. 29B) supplying a current to the EL element (5007), a switching transistor (i.e. switching transistor connected to El element 5007) supplying, to the driver transistor, a signal applied to a source signal line, and a capacitor (capacitor at 5004, Fig. 29B) placed between a gate terminal of the driver transistor and an output terminal of the switching
transistor (column 34, lines 38-65, column 35, lines 5-22).

(5) Regarding claim 20:

Yamazaki ('4887) further discloses wherein the pixel includes a driver transistor (5005, Fig. 29c) supplying a current to the EL element (5007), and

a switching transistor (switching transistor corresponding to the EL element) on a current path, and the current is controlled by turning on and off the switching transistor to generate strip-like non-display areas and strip-like display areas in a display screen (see the illustration in Fig. 27 for stripe like display are)(column 31, lines 30-50, column 32, lines 6-25).

(6) Regarding claim 21:

Yamazaki ('4887) further discloses wherein a display screen is configured with red pixels, green pixels, blue pixels and white pixels, each being arranged in a matrix (column 32, lines 42-45).

5. Claims 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Tam as applied to claim10 above, and further in view of Miyazima (US Pub. No: 2002/0171086 A1)

(1) Regarding claim 11:

Note that Yamazaki ('4887) teaches a first wiring (i.e. data line or source line), but Yamazaki does not teach the first wiring has a light shielding function.

However, Miyajima in the same field of endeavor teaches a first wiring (i.e. data line) has a light shielding function [0036], [0127].

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of first wiring (i.e. data line) comprised a light shielding function as taught by Miyajima in to the El display system of Yamazaki as modified by Tam so that the first wiring could have a shielding function. In this configuration the system would provide a high quality EL display panel with high resolution and improved reliability (Miyajima, [0004]).

(2) Regarding claim 17:

Note that Yamazaki ('5549) does not disclose wherein the supply line is arranged to perform a light-shielding function for a circuit forming section of the driver IC chip.

However, Miyajima in the same field of endeavor teaches a supply line (i.e. supply line corresponding to data line) is arranged to perform a light-shielding function for a circuit forming section of the driver IC chip [0036], [0127].

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of supply line as taught by Miyajima in to the El display system of Yamazaki ('4887) as modified by Yamazaki ('5549) so that the supply line could be arranged to perform a light-shielding function for a circuit forming section of the driver IC chip. In this configuration the system would provide a high quality EL display panel with high resolution and improved reliability (Miyajima, [0004]).

Response to Arguments

6. Applicant's arguments with respect to claims 1 have been considered but are are moot in view of new ground of rejection.

In view of amendments the reference of Yamazaki (US Patent No: 6274887 A1) has been added for further consideration.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Shaheda Abdin whose telephone number is (571) 270-1673.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard HJerpe could be reached at (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pari-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shaheda Abdin

12/15/2009

/Richard Hjerpe/

Supervisory Patent Examiner, Art Unit 2629